Skywire® Nano
Hardware Design Checklist

NimbeLink Corp.
Updated: February 2021

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1. Introduction

1.1 Scope

This document serves as a hardware design checklist for customers who are integrating NimbeLink's Skywire Nano modems into their products. Included in this document is a checklist of important design considerations, as well as suggestions and tips for improving designs utilizing Skywire Nano modems.

1.2 Orderable Part Numbers

Orderable Device	Operating Temperature	4G LTE-M Bands	4G LTE NB-IoT Bands
NL-SWN-LTE-NRF9160	-40℃ to +85℃	B1, B2, B3, B4, B5, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B66	B1, B2, B3, B4, B5, B8, B12, B13, B17, B19, B20, B25, B26, B28, B66
NL-SWN-LTE-NRF9160-B			

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2. Design Checklist

2.1 Pin Types

The table below contains a legend for the abbreviations used for the pin types throughout this document:

Pin Type	Description
PI	Power Input
PO	Power Output
AI	Analog Input
DI	Digital Input
DO	Digital Output
IO	Digital Input/Output

2.2 Pin Implementation Considerations

The table below contains a list of requirements and recommendations for each of the pins on the Skywire Nano modem.

"Design Requirements" are critical implementation steps that must be followed at all times. Any row that is marked with "**Required**" is one of these critical implementation steps.

"Design Recommendations" are optional implementation steps that are strongly suggested. These suggestions can help to improve modem functionality and reduce power consumption, among other things. Any row that is marked with "**Suggested**" is one of these recommendations.

Please refer to the Skywire Nano datasheet for additional design considerations and general information for the modem:

https://nimbelink.com/Documentation/Skywire/Nano/4G_LTE_Cat_M1_Nordic/1002347_NL-SWN-LTE-NRF9160_Datasheet.pdf

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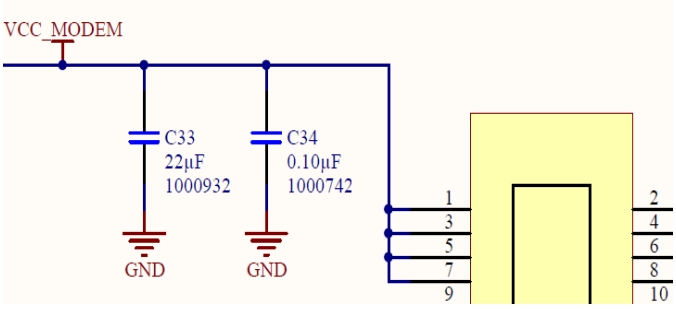
Pin	Pin Name	Type	Level	Notes	Done?
1, 3, 5, 7	VCC	PI	Pins 1, 3, 5, 7 are the main power supply input pins for the modem.		
			Required	The design employs one of the following to supply power to the modem: • Standard 5V 500mA USB bus power. • Switching regulator with a switching frequency of at least 1MHz. • LDO with a fast transient response (1A/µs). • A battery with accompanying SoC monitoring and voltage regulation. A 3.6V Li-Ion battery with at least 1Ah of capacity is recommended.	☐
				The power supply can source enough current to ensure that the VCC rail remains within the recommended operating voltage range with minimal voltage drooping.	☐
				The power supply's output voltage does not drop outside of the modem's operating voltage range at any time during modem operation.	☐
				The power supply has a rapid transient response that can support sudden current spikes during LTE operation.	☐
				Appropriate low-ESR decoupling capacitors have been added for the VCC pins. • A 100 nF capacitor placed nearest to the VCC pins, followed by a 22 µF capacitor is recommended.	☐

The image below is from the NL-SWNDK schematic, and shows a satisfactory selection of decoupling capacitors for the VCC pins:



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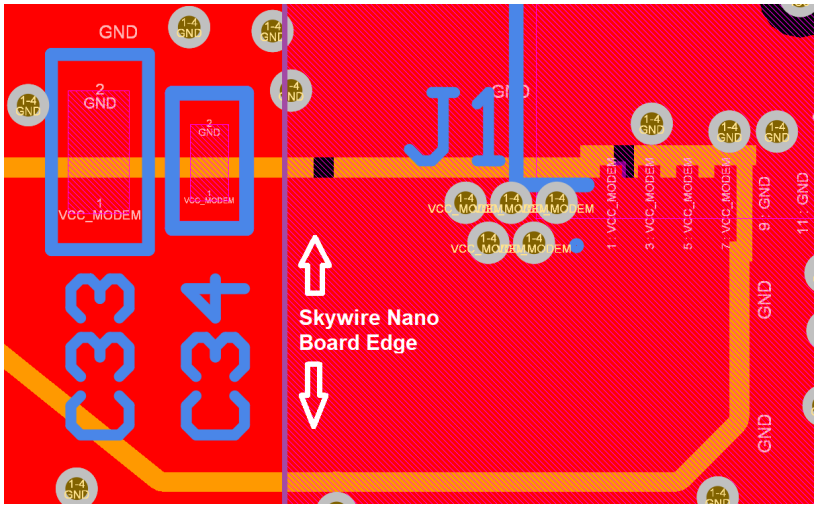
Pin	Pin Name	Type	Level	Notes	Done?
1, 3, 5, 7	VCC	PI	**Required**	The decoupling capacitors are placed directly in the power path.	☐
				No decoupling or bypass capacitors are placed underneath the modem.	☐
				The PCB traces from the power supply are wide enough to ensure that there is a low impedance power delivery path to the modem. • A minimum trace width of 80 mils is recommended.	☐
				Any power traces/pours that transition between PCB layers have multiple vias. • It is recommended to use at least 4 vias for each trace that transitions across PCB layers.	☐
				The VCC pins have continuous connections to the power plane/traces. Thermal reliefs are not used on any pins.	☐
				Noise sensitive signal lines (such as USB or RF signals) are kept away from the power supply traces and cables.	☐

The image below is from the NL-SWNDK layout, and depicts a satisfactory implementation of the decoupling capacitors and VCC pins:



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Pin	Pin Name	Type	Level	Notes	Done?
1, 3, 5, 7	VCC	PI	Suggested	There exists a way to disconnect the VCC pins from the power supply when the modem is powered off. • This allows the modem to achieve the lowest possible quiescent current consumption.	☐
2, 9, 11, 13, 15, 25, 27, 28, 37, 42, 59, 60	GND	PI	Required	All of the modem's GND pins have been connected to system GND.	☐
				No thermal reliefs have been used to connect to the modem's GND pins.	☐
				Unused space on signal layers is flooded with GND and connected to the GND plane with numerous stitching vias. • Stitching vias should be placed roughly every 150 mils for ideal grounding.	☐
			Suggested	A 4 layer PCB with a dedicated GND plane is strongly recommended.	☐
4, 6, 8, 12, 14,16, 18, 20, 22, 24, 26, 30, 31, 34, 36, 38, 39, 40, 41, 43, 45, 47	IOx	IO	Digital I/O pins are **optionally connected** depending on the user's design requirements.		
			Required	All unused IO pins are set as outputs and driven low.	☐
			Suggested	The signal(s) applied to each input pin fall within the acceptable input voltage range.	☐
				All input/output pins are only expected to sink/source up to 4mA of current.	☐
10	IO5	IO	IO5 can be used to force NL-SWN-LTE-NRF9160-B modems into Device Firmware Upgrade (DFU) mode during the boot process. This serves as a recovery mode in the event that the application firmware becomes unstable or for general firmware flashing.		
			Required	IO5 is not asserted during modem boot when the device is operating normally. • IO5 can be used as a normal GPIO pin **after the modem has booted.** See Section 4.12.2 in the Skywire Nano Datasheet for more info.	☐

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Pin	Pin Name	Type	Level	Notes	Done?
10	IO5	IO	Suggested	There exists a way to enter DFU mode by tying IO5 to VCC_GPIO before modem boot.	☐
				The signal(s) applied to IO5 fall within the acceptable input voltage range.	☐
				IO5 is only expected to sink/source up to 4mA of current.	☐
17	nRESET	DI	Pin 17 is used to reset the modem and to wake it up from the powered off state. It must be implemented.		
			Required	Pin 17 driven with an open-drain output on the host processor, reset button, etc.	☐
				Pin 17 is never pulled up or driven high by the baseboard.	☐
19	ENABLE	DI	Pin 19 is the ENABLE signal, and is used to turn the modem on. It must be asserted to VCC in order to boot the modem.		
			Required	Pin 19 is implemented and there exists a way to assert a high state on this pin.	☐
				Pin 19 is driven with an output pin on the host controller, pulled up to VCC with a 10k resistor, or some equivalent method.	☐
			Suggested	If hardware permits, there exists a way to ground pin 19 when the modem is off. • This allows for the lowest possible quiescent current consumption for the modem.	☐
21, 23	VCC_GPIO	PI	Pins 21 and 23 serve as the GPIO reference voltage and power supply input pins for the Skywire Nano.		
			Required	The chosen power supply for VCC_GPIO can source enough current to meet the needs of the GPIO pin implementation.	☐
				If the VCC_GPIO and VCC rails share the same power supply, special care has been taken to ensure that the two rails do not exceed the output current limit of the power supply at any time.	☐

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Pin	Pin Name	Type	Level	Notes	Done?
21, 23	VCC_GPIO	PI	Suggested	If the GPIO pins are sourcing a significant amount of current, appropriate low-ESR decoupling capacitors have been placed as close as possible to the VCC pins. • It is recommended to use a 22uF and a 100nF capacitor.	☐
			Required	No decoupling or bypass capacitors are placed underneath the modem.	☐
				The PCB traces from the power supply are wide enough to ensure that there is a low impedance power delivery path to the modem's VCC_GPIO pins. • A minimum trace width of 30 mils is recommended.	☐
29	EXT_VCC_SIM	PO	Pin 29 is the VCC_SIM pin for the optional external SIM interface.		
			Suggested	A compatible SIM has been chosen, such as a 3FF SIM slot, eSIM, or soldered-down SIM.	☐
				Pin 29 is connected to the VCC input of the SIM interface on the baseboard.	☐
				If the SIM card will be accessed in a non-ESD controlled environment, it is strongly recommended to use an ESD protection IC. • The NL-SWNDK reference design uses the Texas Instruments TPD3F303.	☐
				Appropriate bypass capacitors in the pF range are placed near the J1 connector and baseboard SIM IC/connector. • This may be omitted if using an ESD protection IC with EMI filtering.	☐
				The PCB traces are wide enough to ensure that there is a low impedance power delivery path to the external SIM_VCC pin. • A min trace width of 15 mils is ideal.	☐

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Pin	Pin Name	Type	Level	Notes	Done?
29	EXT_VCC_SIM	PO	Suggested	**If Not Implemented:** Pin 29 is connected to a non-populated (NP) SIM card cage or to test points to allow for debugging and testing with an external SIM.	☐
31	EXT_SIM_RST	DO	Pin 31 is the SIM_RST pin for the optional external SIM interface.		
			Suggested	Pin 31 is connected to the reset input of the SIM interface on the baseboard.	☐
				If Not Implemented: Pin 31 is connected to a non-populated (NP) SIM card cage or to test points to allow for debugging and testing with an external SIM.	☐
33	EXT_SIM_IO	IO	Pin 33 is the SIM_IO pin for the optional external SIM interface.		
			Suggested	Pin 33 is connected to the bidirectional I/O pin of the SIM interface on the baseboard.	☐
				Special care has been taken to ensure the signal integrity of this pin. Failure to follow the signal integrity guidelines below may render the external SIM interface inoperable: • The EXT_SIM_IO trace and its associated return current path are as short as possible. • The EXT_SIM_IO signal does not cross any splits in its reference plane. • The EXT_SIM_IO trace is ideally routed on one layer. Otherwise, the usage of vias to change layers is minimized (one or two). • Any filtering capacitors for this signal are placed as close as possible to the external SIM.	☐
				If Not Implemented: Pin 33 is connected to a non-populated (NP) SIM card cage or to test points to allow for debugging and testing with an external SIM.	☐

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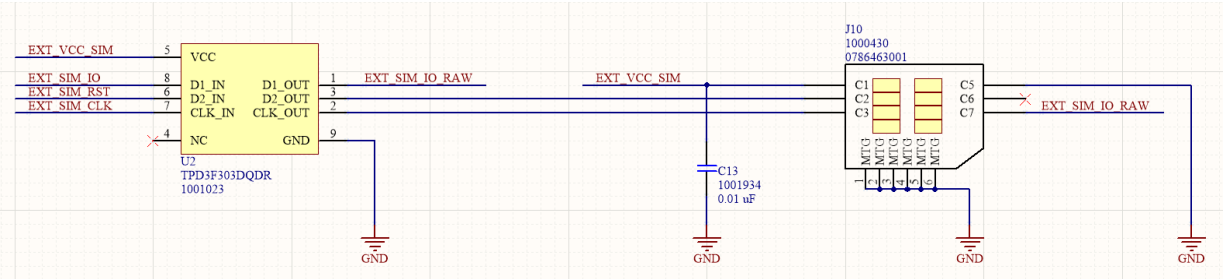
<table>
<tr><th>Pin</th><th>Pin Name</th><th>Type</th><th>Level</th><th>Notes</th><th>Done?</th></tr>
<tr><td rowspan="3">35</td><td rowspan="3">EXT_SIM_CLK</td><td rowspan="3">DO</td><td colspan="3">Pin 35 is the SIM_CLK pin for the optional external SIM interface.</td></tr>
<tr><td rowspan="2">Suggested</td><td>Pin 35 is connected to the bidirectional I/O pin of the SIM interface on the baseboard.</td><td>☐</td></tr>
<tr><td>Special care has been taken to ensure the signal integrity of this pin.

Failure to follow the signal integrity guidelines below may render the external SIM interface inoperable:

• The EXT_SIM_CLK trace and its associated return current path are as short as possible.

• The EXT_SIM_CLK signal does not cross any splits in its reference plane.

• The EXT_SIM_CLK trace is ideally routed on one layer. Otherwise, the usage of vias to change layers is minimized (one or two).

• Any filtering capacitors for this signal are placed as close as possible to the external SIM.</td><td>☐</td></tr>
<tr><td>35</td><td>EXT_SIM_CLK</td><td>DO</td><td>Suggested</td><td>If Not Implemented: Pin 33 is connected to a non-populated (NP) SIM card cage or to test points to allow for debugging and testing with an external SIM.</td><td>☐</td></tr>
<tr><td colspan="6">The images below are from the NL-SWNDK schematic and layout, and depict a satisfactory implementation of the external SIM interface and ESD protection IC:
 
</td></tr>
</table>

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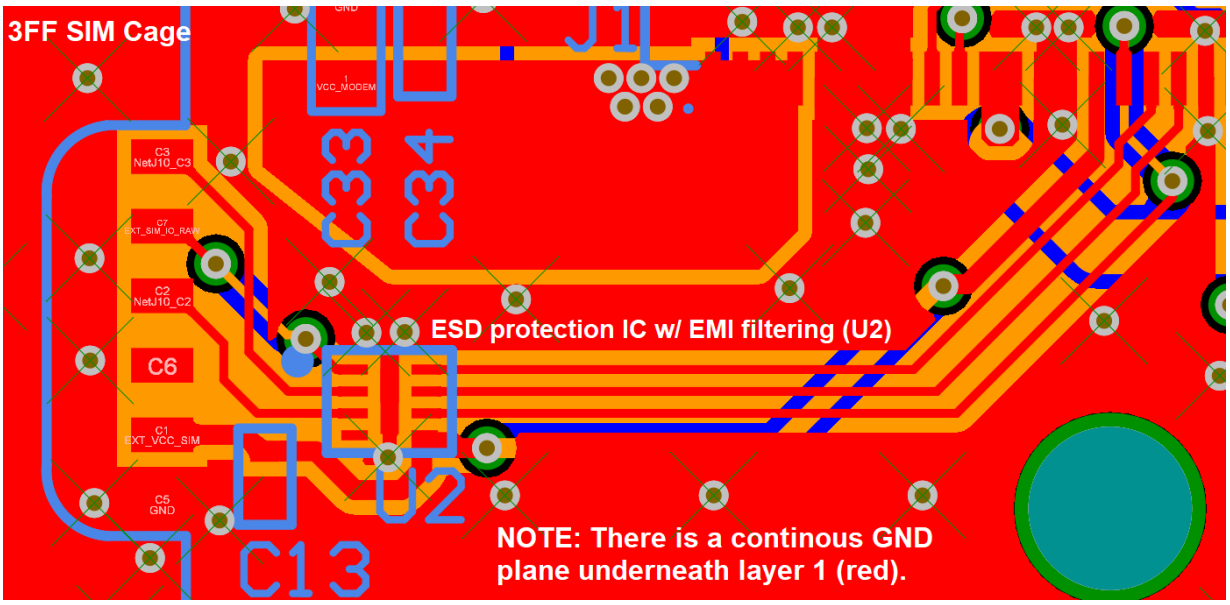

Pin	Pin Name	Type	Level	Notes	Done?
44	IO0_UART1_RX	DI	UART1 is the main communication path for the Skywire Nano, with support for hardware flow control and speeds up to 1M baud. **Pin 44 must be connected.**		
			Required	Pin 44 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐
				The output voltage range of the other UART device is compatible with pin 44 (between 0V and VCC_GPIO).	☐
46	IO1_UART1_TX	DO	UART1 is the main communication path for the Skywire Nano, with support for hardware flow control and speeds up to 1M baud. **Pin 46 must be connected.**		
			Required	Pin 46 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐
				The output voltage range of pin 46 is compatible with the input voltage range of the other UART device.	☐
48	IO14_UART1 _RTS_AIN1	DO	UART1 is the main communication path for the Skywire Nano, with support for hardware flow control and speeds up to 1M baud. **Pin 48 must be connected in order to use flow control.**		
			Suggested	Pin 48 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐

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Pin	Pin Name	Type	Level	Notes	Done?
48	IO14_UART1_RTS_AIN1	DO	Suggested	The output voltage range of pin 48 is compatible with the input voltage range of the other UART device.	☐
				If Not Implemented: Pin 48 is optionally connected to a test point or NP debug header. Otherwise it is left floating.	☐
50	IO15_UART1_CTS_AIN2	DI	UART1 is the main communication path for the Skywire Nano, with support for hardware flow control and speeds up to 1M baud. **Pin 50 must be connected in order to use flow control.**		
			Suggested	Pin 48 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐
				The output voltage range of the other UART device is compatible with pin 50 (between 0V and VCC_GPIO).	☐
				If Not Implemented: Pin 50 is connected to GND through a 10k resistor. Optionally connected to a test point or NP debug header (in addition to the resistor).	☐
52	IO28_UART0_RX	DI	UART0 is used by the modem to output debugging information and perform serial DFU firmware updates. It is strongly recommended to implement UART0, but not strictly required.		
			Suggested	Pin 52 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐
				The output voltage range of the other UART device is compatible with pin 52 (between 0V and VCC_GPIO).	☐
				If Not Implemented: Pin 52 is optionally connected to a test point or NP debug header. Otherwise it is left floating.	☐
54	IO29_UART0_TX	DO	UART0 is used by the modem to output debugging information and perform serial DFU firmware updates. It is strongly recommended to implement UART0, but not strictly required.		
			Suggested	Pin 54 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐

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Pin	Pin Name	Type	Level	Notes	Done?
54	IO29_UART0_TX	DO	Suggested	The output voltage range of pin 54 is compatible with the input voltage range of the other UART device.	☐
				If Not Implemented: Pin 54 is optionally connected to a test point or NP debug header. Otherwise it is left floating.	☐
56	IO27_UART0_RTS	DO	UART0 is used by the modem to output debugging information and perform serial DFU firmware updates. It is strongly recommended to implement UART0, but not strictly required. The use of flow control during DFU updates is strongly recommended to maximize update speed.		
			Suggested	Pin 56 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐
				The output voltage range of pin 56 is compatible with the input voltage range of the other UART device.	☐
				If Not Implemented: Pin 56 is optionally connected to a test point or NP debug header. Otherwise it is left floating.	☐
58	IO26_UART0_CTS	DI	UART0 is used by the modem to output debugging information and perform serial DFU firmware updates. It is strongly recommended to implement UART0, but not strictly required. The use of flow control during DFU updates is strongly recommended to maximize update speed.		
			Suggested	Pin 58 is connected to a UART peripheral, USB-UART converter, debug header, etc.	☐
				The output voltage range of the other UART device is compatible with pin 58 (between 0V and VCC_GPIO).	☐
				If Not Implemented: Pin 58 is connected to GND through a 10kΩ resistor. Optionally connected to a test point or NP debug header (in addition to the resistor).	☐

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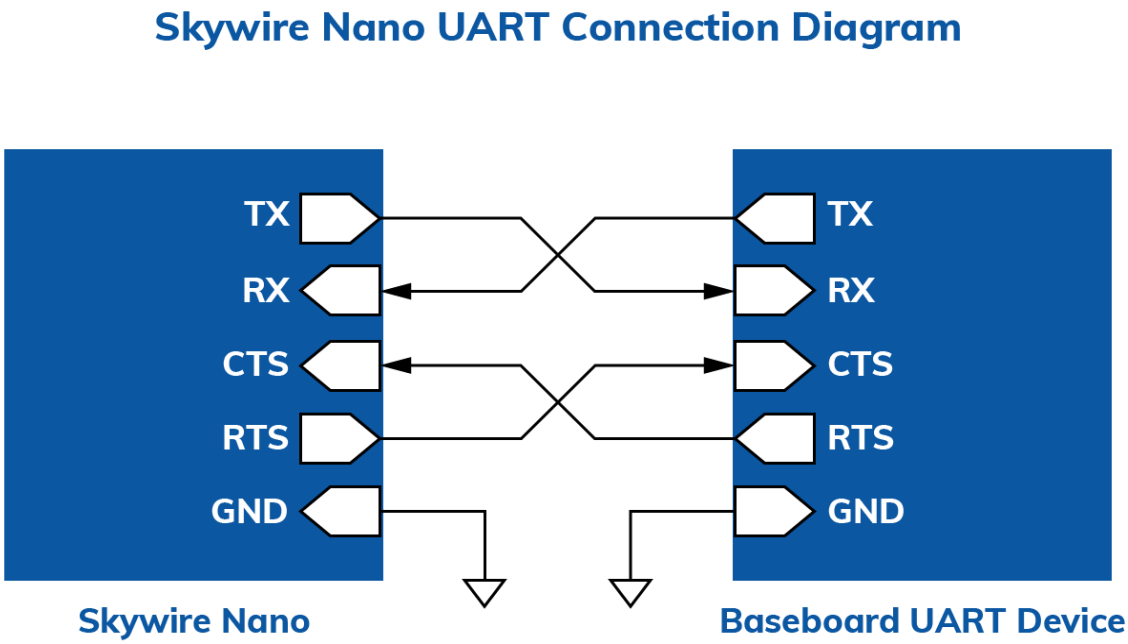
The image below is taken from the Skywire Nano Datasheet, and depicts the directions of the UART0 and UART1 signals, and how to properly connected them to another UART device:



Pin	Pin Name	Type	Level	Notes	Done?
49, 51, 53	MAGPIO	DO		The MAGPIO pins are used to control antenna tuning circuitry on the baseboard. These pins should only be implemented by advanced users for designs that make use of an RF switch and multiple antenna matching networks to dynamically tune the modem's antenna.	
			Suggested	The chosen RF switch is compatible with the MAGPIO interface.	☐
			Suggested	Manufacturer layout guidelines were followed when implementing the RF switch and antenna matching networks.	☐
			Required	Pins 49, 51 and 53 are left floating if unused.	☐
55	SWDCLK	DI		Pin 55 is the SWDCLK signal for the modem and can be used to flash application code onto the modem and debug. Pin 55 must be implemented.	
			Required	Pin 55 is wired to a debug connector for interfacing with an SWD debugger. Otherwise, this pin is connected to a test point or NP header.	☐

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<table>
<tr><th>Pin</th><th>Pin Name</th><th>Type</th><th>Level</th><th>Notes</th><th>Done?</th></tr>
<tr><td>55</td><td>SWDCLK</td><td>DI</td><td>Required</td><td>Special care has been taken to ensure the signal integrity of this pin.

Failure to follow the signal integrity guidelines below may render the SWD interface inoperable:
The SWDCLK trace and its associated return current path are as short as possible.
The SWDCLK signal does not cross any splits in its reference plane.
The SWDCLK trace is ideally routed on one layer. Otherwise, the usage of vias to change layers is minimized (one or two).</td><td>☐</td></tr>
<tr><td rowspan="3">57</td><td rowspan="3">SWDIO</td><td rowspan="3">IO</td><td colspan="3">Pin 57 is the SWDCLK signal for the modem and can be used to flash application code onto the modem and debug. Pin 55 must be implemented.</td></tr>
<tr><td rowspan="2">Required</td><td>Pin 57 is wired to a debug connector for interfacing with an SWD debugger. Otherwise, this pin is connected to a test point or NP header.</td><td>☐</td></tr>
<tr><td>Special care has been taken to ensure the signal integrity of this pin.

Failure to follow the signal integrity guidelines below may render the SWD interface inoperable:
The SWDIO trace and its associated return current path are as short as possible.
The SWDIO signal does not cross any splits in its reference plane.
The SWDIO trace is ideally routed on one layer. Otherwise, the usage of vias to change layers is minimized (one or two).</td><td>☐</td></tr>
</table>

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2.3 Power Supply Considerations

Design Considerations	Done?
The power supply layout is in accordance with the manufacturer's guidelines.	☐
Power supply switching current loops are minimized, if applicable.	☐
The power supply is controlled in a manner such that the power will not be cut from the modem until the modem has properly shut down.	☐
A mechanism is implemented that ensures the modem can always gracefully disconnect from the network in the event of a power failure.	☐

2.4 Antenna Considerations

Design Considerations	Done?
An appropriate primary cellular antenna has been selected for the modem. • Refer to the Skywire Nano datasheet for antenna design requirements and recommended antennas. • A wide-band LTE antenna that offers high efficiency across the entire LTE spectrum is ideal.	☐
If GPS is used in the design, an appropriate GPS antenna has been selected for the modem. • Refer to the Skywire Nano datasheet for antenna design requirements and recommended antennas.	☐
The cellular and GPS antennas are sufficiently isolated from noise generated by other design components.	☐
The cellular and GPS antennas are mounted in accordance with the manufacturer's guidelines.	☐

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2.6 Enclosure Considerations

Design Considerations	Done?
The enclosure design insulates the Skywire Nano from outdoor environments. • A sealed enclosure is recommended.	☐
The enclosure design ensures that the Skywire Nano is protected from moisture. • Condensing moisture may permanently damage the modem. Check the modem datasheet for acceptable humidity ranges.	☐
The enclosure design ensures that the Skywire Nano is protected from extreme temperatures. • Extreme temperatures may permanently damage the modem. Check the modem datasheet for acceptable operating and storage temperature ranges.	☐
The enclosure does not adversely affect the signal strength of the antenna(s). • Metal enclosures and metal objects will block and/or detune antenna systems. Consult an RF engineer for guidance on antenna selection and placement.	☐

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3. Document Version Information

Revision	Author	Description	Date
1	SR	Initial document release.	02/18/21

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